

| PIN | CONNECTION | PIN | CONNECTION |
| :---: | :---: | :---: | :---: |
| 1 | +5 V | 22 | +28 V |
| 2 | Output 1 Noninv | 21 | Input 4A |
| 3 | Input 1 | 20 | Input 4B |
| 4 | Output 1 Inv | 19 | Input 6C |
| 5 | Output 2 Noninv | 18 | NC |
| 6 | Input 2 | 17 | NC |
| 7 | Output 2Inv | 16 | Output 4 Noninv |
| 8 | Output 3 Noninv | 15 | NC |
| 9 | Input 3 | 14 | NC |
| 10 | Output 3 Inv | 13 | NC |
| 11 | Ground | 12 | -3 V |

Notes:

1) Channels 1, 2, and 3 are independent and provide complementary outputs. Logic low on these channel inputs causes the noninverting output of that channel to sink current.
2) Channel 4 has three inputs and one output. If any of the channel 4 inputs are low, the output will sink current. Channel 4 logic inputs do not have active pull-ups, to conserve supply current. The three channel 4 inputs are typically externally connected to the input pins of the three other channels, to provide an OR capability.
3) Outputs are capable of providing up to -100 mA (thru external series resistors) into anode-grounded diodes, or $\mathbf{+ 2 8 V}$ for back-bias of diodes.
4) Switching speed is 10 microseconds maximum.
5) Unit contains internal .01 uF bypass capacitor on +5 V supply and -3 V supply.

External bypassing is recommended on the $\mathbf{+ 2 8 V}$ supply.
6) +5 V and +28 V supply current are each less than 5 mA under the conditions of either all inputs high, or the condition of one channel 4 input low and one of the other channel innuts low.

| $$ | Revisions |  |  |  | Impellimax |  |  |
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|  |  |  |  |  | OUTLINE |  |  |
|  |  |  |  |  |  |  | Sheet 2 of 2 |
|  |  |  |  |  | Drawn By: PC | Date: $3 / 21 / 01$ | Drawing \# |
|  |  |  |  |  | DRF: 551 | Approved: ${ }_{\text {P.c. }}$ | 9691-50 |

