

	Revisions				<u>lmpellimax</u>			
Tolerances Except as Noted	Rev	Number	Date	Ву	OUTLINE			
.x = +/05 .xx = +/01 .xxx = +/005 Dimensions in inches								
					Drawn By: P.C.		Date: 10/2/00	Sheet 1 of 2
Information herein is believed accurate. Suitability not guaranteed.					DRF:	Date:	Approved:	Drawing #
					512	10/2/00	P.C.	NX4-53

PIN	CONNECTION	PIN	CONNECTION
1	Vee	22	NC
2	Output 1	21	Output 4
3	TP 1	20	TP 4
4	NC	19	NC
5	in 1	18	In 4
6	Ground	17	+ 5 V
7	In 2	16	In 3
8	NC	15	NC
9	TP 2	14	TP 3
10	Output 2	13	Output 3
11	NC	12	NC

## Notes:

- 1) Inputs are TTL compatible.
- 2) Channels are independent and noninverting. Logic hi on input causes output to go positive. Logic low on input causes output to go negative.
- 3) Switching speed is 5 to 8 nsec maximum into 1N914 loads.
- 4) Unit contains an internal .01 uF bypass capacitors on both supplies.
- 5) Output testpoints are voltage sources that allow for boosting of steadystate output current, or for alternative spiking circuits.

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