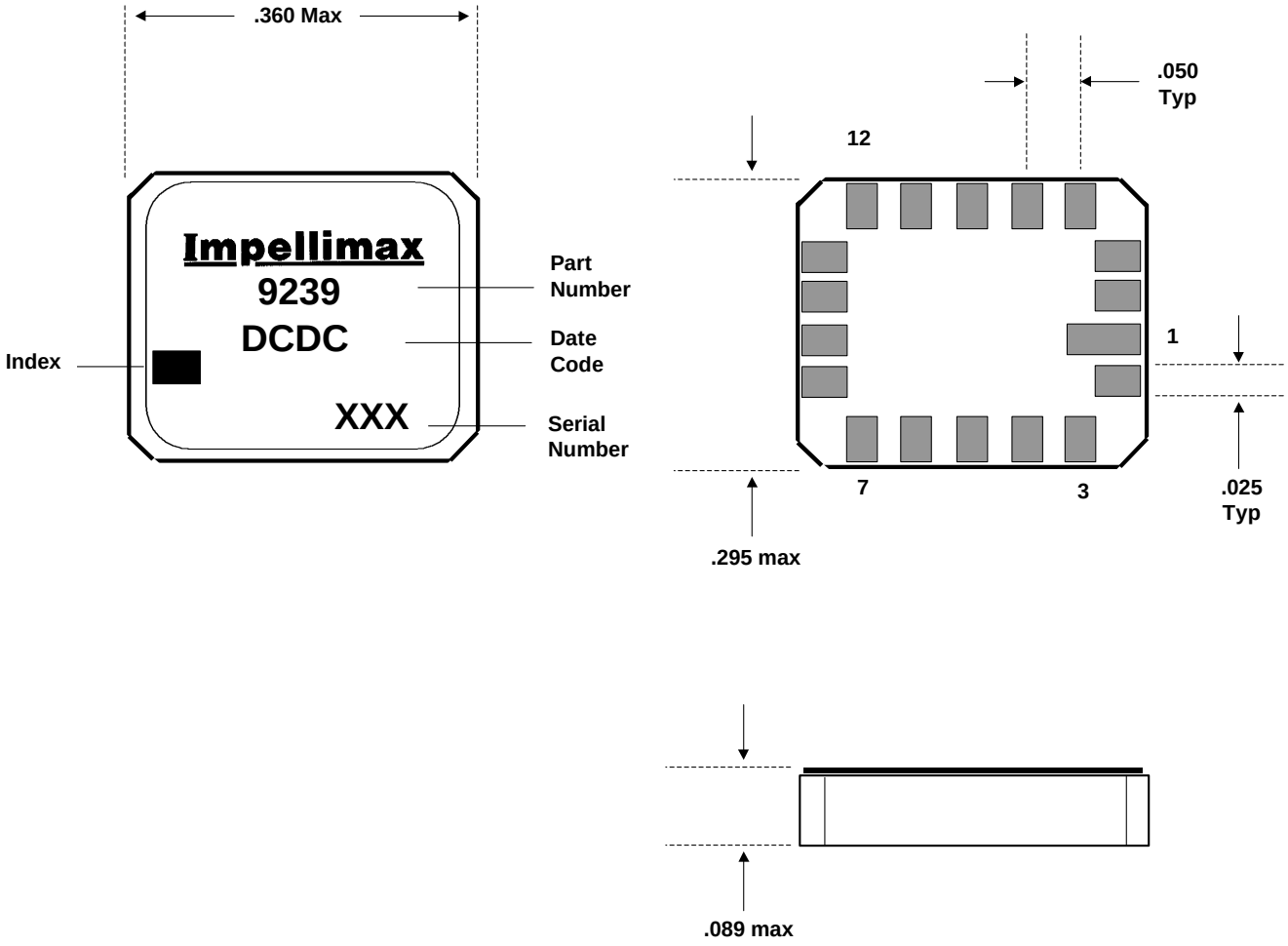

Package Code L

Tolerances Except as Noted .x = +/- .05 .xx = +/- .01 .xxx = +/- .005 Dimensions in inches	Revisions				Impellimax	
					OUTLINE	
						Sheet 1 of 2
Information herein is believed accurate. Suitability not guaranteed.					Drawn By: PC	Date: 5/5/00
					DRF: 467	Approved: PC
						Drawing # 9239-50

PIN	CONNECTION	PIN	CONNECTION
1	- V	18	NC
2	NC	17	Out 1
3	Ground	16	NC
4	TTL IN 1	15	NC
5	NC	14	NC
6	TTL IN 2	13	NC
7	NC	12	NC
8	NC	11	Out 2
9	+ 5 V	10	NC

Notes:

1) Channels are independent and noninverting, compatible with 5V CMOS logic. Logic hi causes output to source curent. Logic low causes output to provide negative voltage for back bias of diodes.

2) Unit does not contain internal supply bypass capacitors.

3) Switching speed negative to positive is 80 nsec max into shunt diode loads.

4) Output current must be externally limited by series resistors. Output current can be in the range of 1 to 60 mA per output.

5) Negative supply voltage can be in the range of -2 to -12 V .

Tolerances Except as Noted .x = +/- .05 .xx = +/- .01 .xxx = +/- .005 Dimensions in inches	Revisions				Impellimax		
					OUTLINE		
							Sheet 2 of 2
Information herein is believed accurate. Suitability not guaranteed.					Drawn By: P.C.	Date: 5/5/00	Drawing # 9239-50
					DRF: 467	Approved: P. C.	