



<p>Tolerances Except as Noted .x = +/- .05 .xx = +/- .01 .xxx = +/- .005 Dimensions in inches</p>	<b>Revisions</b>				<b><u>Impellimax</u></b>		
					<b>OUTLINE</b>		
							Sheet 1 of 2
<p>Information herein is believed accurate. Suitability not guaranteed.</p>					Drawn By: P.C.	Date: 8/25/00	Drawing #
					DRF: 503	Approved: P.C.	<b>9683-50</b>

PIN	CONNECTION	PIN	CONNECTION
1	+ 5 V	22	NC
2	Input A (lsb)	21	Out 1 NI
3	Input B (msb)	20	Out 1 Inv
4	NC	19	Out 2 NI
5	Latch	18	NC
6	Ground	17	Out 2 Inv
7	Bit A out	16	NC
8	Bit B out	15	Out 3 NI
9	NC	14	NC
10	NC	13	Out 3 Inv
11	-5V	12	NC

**Notes:**

- 1) Logic "0" is defined as 0.8 V max, logic "1" is 1.4 to 5 V max. Logic low TTL current is 0.8 mA max. The latch input is edge-triggered and loads the two-bit word from the input pins into the 1 of 3 decoder upon the rising edge of the latch command. Input A and Input B must be stable for at least 50 nsec before the latch command is given.
- 2) When a channel is selected by the internal 1 of 3 decoder, noninverting outputs provide +30 mA positive current and inverting outputs provide -30 mA negative current. Outputs switch states when deselected.
- 3) Switching speed is 2 microseconds max.
- 4) Unit contains 2N2222A and 2N3906 transistors as the only active device types. Unit contains only 33 pF ceramic capacitors and thin-film substrate resistors as passive elements.
- 5) Bit A Out and Bit B Out pins provide logic status following the latch. These bits therefore asynchronously mimic the internal logic that is being applied to the 1 of 3 decoder stage.

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