

| PIN | CONNECTION | PIN | CONNECTION |
| :---: | :---: | :---: | :---: |
| 1 | Output 1 | 22 | Input 1 |
| 2 | Output 2 | 21 | Input 2 |
| 3 | Output 3 | 20 | Input 3 |
| 4 | Output 4 | 19 | Input 4 |
| 5 | Output 5 | 18 | Input 5 |
| 6 | Output 6 | 17 | Input 6 |
| 7 | Ground | 16 | LNA Control Input |
| 8 | Ground | 15 | + 3.3 V |
| 9 | Ground | 13 | +11 V V |
| 10 | LNA Output | 12 | LNA Testpoint 2 |
| 11 | CNA |  |  |

Notes:

1) Steady-state output current capability of PIN channels is + $\mathbf{3 0} \mathrm{mA}$ minimum. Output current is set by external resistors. Current spikes are determined by external capacitors in parallel with these resistors. Negative output is for backbias only.
2) PIN channels switching speed is 8 nsec max loaded with a shunt 1N914 diode. Output current for this test is $\mathbf{3 0} \mathbf{~ m A}$ nominal.
3) LNA channel switching speed is 10 nsec. LNA Testpoints are adjusted with external resistors to ground,typically with 390 ohms on TP 1 and 270 ohms on TP 2. Expected output voltages for the LNA channel are -.54V and -1.5 V.
4) Unit contains internal .01 uF bypass capacitors on both power supplies.
5) PIN Driver channels are independent and inverting. LNA channel logic is TBD.

| Tolerances Except as Noted$\begin{aligned} & . \mathrm{x}=+/- .05 \\ & . \mathrm{xx}=+/- \\ & .01 \\ & . \mathrm{xxx}=+/- \\ & \text { Dimensions } \\ & \text { in inches } \end{aligned}$ | Revisions |  |  |  | Impelimax |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | A | ECO 1994 | 3/2/2000 | PC | OUTLINE |  |  |
|  | B | ECO 2086 | 10/29/00 | PC |  |  |  |
|  |  |  |  |  |  |  | Sheet 2 of 2 |
| Information herein is believed accurate. Suitability not guaranteed. |  |  |  |  | Drawn By: ${ }_{\text {P.C. }}$ | $\text { Date: }{ }_{2 / 11 / 00}$ | Drawing \# 9713-50 |
|  |  |  |  |  | DRF: 433 | Approved: P . C. |  |

