

| PIN | CONNECTION | PIN | CONNECTION |
| :---: | :---: | :---: | :---: |
| 1 | +5 V | 22 | NC |
| 2 | AO Input | 21 | Switch 1-1 (A) |
| 3 | A1 Input | 20 | Switch 1-2 (D) |
| 4 | NC | 19 | Switch 2-1 (F) |
| 5 | NC | 18 | NC |
| 6 | Ground | 17 | Amp 1 (B) |
| 7 | NC | 16 | NC |
| 8 | NC | 15 | Amp 2 (E) |
| 9 | NC | 14 | NC |
| 10 | NC | 13 | Switch 2-2 (H) |
| 11 | -5 V | 12 | DRO (C) |
|  |  |  |  |

Notes:

1) Logic inputs A0 and A1 are compatible with CMOS outputs and require pull-ups if operated with bipolar TTL outputs.
2) Switch outputs swing between +4.5 V and -4.5 V minimum. Output current, in the range of $\mathbf{1}$ to $\mathbf{2 5} \mathbf{~ m A}$, is to be set by external series resistors. Amplifier and DRO outputs are not current limited and do not actively pull down to ground.
3) Switch speed is $\mathbf{2}$ microseconds typical, $\mathbf{8}$ microseconds maximum.
4) Unit contains internal .01 uF bypass capacitors on both power supplies.
5) Supply current, exclusive of load current, is $+/-10 \mathrm{~mA}$ max when operated at $+/-5 \mathrm{~V}$ at low PRF.

| Band | Control Line |  | Switch1- |  | Switch1-2 |  | Switch2-1 |  | Amp 1 |  | Amp 2 |  | Switch2-2 |  | DRO |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Conn Pt | 5 | 3 | A |  | D |  | F |  | B |  | E |  | H |  | C |  |
| $\mathrm{V} / \mathrm{I}$ | A1 | A0 | V | mA | V | mA | V | mA |  | mA | V |  | V | A |  | A |
| X Band | 0 | 0 |  | +20 |  | -20 |  | +20 | +5 | +24 | 0 | 0 | -5 | -20 | 0 | 0 |
| K Band | 0 | 1 | -5 | -20 | +5 | +20 | +5 | +20 | +5 | +24 | +5 | +24 | +5 | +20 | +5 | +25 |
| S Band | 1 | 0 |  | +20 | -5 | -20 | -5 | -20 | +5 | +24 | 0 | 0 | +5 | +20 | +5 | +25 |
| X Bnd tst | 1 | 1 | +5 | +20 | +5 | +20 | +5 | +20 | 0 | 0 | 0 | 0 | +5 | +20 | 0 | 0 |



