

	Tolerances Except as Noted	Revisions				<u>lmpellimax</u>			
	.x = +/05 .xx = +/01 .xxx = +/005 Dimensions in inches					OUTLINE			
									Sheet 1 of 2
	Information herein is believed accurate. Suitability not					Drawn	By: P. C.	Date: 8/25/00	Drawing #
	guaranteed.					DRF:	502	Approved: P. C.	TS3-50

PIN	CONNECTION	PIN	CONNECTION
1	-5 V to -12V	22	NC
2	NC	21	Out 1 NI
3	NC	20	Out 1 Inv
4	Ground	19	Out 2 NI
5	In 1	18	Out 2 Inv
6	ln 2	17	Out 3 NI
7	In 3	16	Out 3 Inv
8	NC	15	NC
9	NC	14	NC
10	NC	13	NC
11	+5V	12	NC

Notes:

- 1) Channels are independent and TTL compatible. Logic "0" is defined as 0.8 V max, logic "1" is 1.4 to 5 V max. Logic low TTL current is 0.5 mA max.
- 2) For input Hi, noninverting outputs provide positive current and inverting outputs provide negative voltage. Outputs switch states for logic low input.
- 3) Switching speed is 60 nsec max.
- 4) Unit contains internal .01 uF bypass capacitors.
- 5) For TS399xx family, outputs are not current limited. Use external resistors to limit positive output current to 15 mA max. Negative outputs are for back bias only.

Tolerances Except as Noted	Revisions				<u>Impellimax</u>					
.x = +/05 .xx = +/01 .xxx = +/005 Dimensions in inches						OUTLINE				
								Sheet 2 of 2		
Information herein is believed accurate. Suitability not					Drawn	By: P. C.	Date: 8/25/90	Drawing #		
guaranteed.					DRF:	502	Approved: P. C.	TS3-50		